Notice of Allowability	Application No.	Applicant(s)	
	10/706,162	NEMATI ET AL.	
	Examiner	Art Unit	
	Jerome Jackson Jr.	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Board of Appeals decision*.

2. ☒ The allowed claim(s) is/are *3-5,7-14,16-18,23,25*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Cancel claims 1, 2, 6, 15, 19-22, 24 and 26.

Rewrite allowed claims 3, 4, 7, 11, 16 and 18 as follows:

3. A semiconductor device comprising:

a thyristor having thyristor body regions including first and second immediately adjacent base regions between first and second emitter regions;

a first control port configured and arranged to capacitively couple a first signal at least to the first base region;

and a second control port configured and arranged for receiving a second signal generated outside of the thyristor and for coupling the second signal at least to the second base region, the second signal being adapted to control holding current or forward blocking voltage of the thyristor as a function of temperature;

a circuit arrangement electrically coupled to the second control port and configured and arranged to apply the second signal to the second control port;

wherein the circuit arrangement includes a temperature sensing circuit electrically coupled to the thyristor and configured and arranged to apply the second signal to the second control port as a function of the temperature of the thyristor.

4. The semiconductor device of claim 3, wherein the second signal applied by the temperature sensing circuit is adapted to increase bipolar gains of the thyristor when the temperature of the thyristor is below a selected threshold.

7. A memory device comprising:

at least one thyristor having thyristor body regions including first and second immediately adjacent base regions respectively coupled to and between first and second emitter regions;

a first control port configured and arranged to capacitively couple a first signal at least to the first base region;

a first circuit configured and arranged to detect a temperature-related failure of the thyristor to maintain its conductance state during a standby mode or to maintain its blocking state;

and a second circuit including a second control port configured and arranged for receiving a second signal generated outside of the thyristor and for coupling the second signal at least to the second base region as a function of the detected failure for controlling holding current or forward blocking voltage of the thyristor;

further comprising a reference thyristor, the first circuit being configured and arranged to detect the failure condition from the reference thyristor.

11. A memory device comprising:

at least one thyristor having thyristor body regions including first and second immediately adjacent base regions respectively coupled to and between first and second emitter regions;

a first control port configured and arranged to capacitively couple a first signal at least to the first base region;

a first circuit configured and arranged to detect a temperature-related failure of the thyristor to maintain its conductance state during a standby mode or to maintain its blocking state;

a second circuit including a second control port configured and arranged for receiving a second signal generated outside of the thyristor and for coupling the second signal at least to the second base region as a function of the detected failure for controlling holding current or forward blocking voltage of the thyristor;

further comprising a plurality of memory cells, each memory cell including a thyristor, wherein the first circuit further comprises:

a first reference memory cell including a thyristor and adapted to store a data "zero" and to fail to retain the data "zero" as a function of the conductance state of the thyristor in the first reference memory cell before other memory cells in the memory device fail data "zero";

a second reference memory cell including a thyristor and adapted to store a data "one" and to fail to retain the data "one" as a function of the conductance state of the thyristor in the second reference memory cell before other memory cells in the memory device fail data "one";

and the second circuit being adapted to apply the second signal to the second control port as a function of at least one of the first and second reference memory cells failing to retain data.

16. A memory device comprising:

at least one thyristor having thyristor body regions including first and second immediately adjacent base regions respectively coupled to and between first and second emitter regions;

a first control port configured and arranged to capacitively couple a first signal at least to the first base region;

a first circuit configured and arranged to detect a temperature-related failure of the thyristor to maintain its conductance state during a standby mode or to maintain its blocking state;

and a second circuit including a second control port configured and arranged for receiving a second signal generated outside of the thyristor and for coupling the second signal at least to the second base region as a function of the detected failure for controlling holding current or forward blocking voltage of the thyristor;

wherein the second control port extends over a junction between the second base region and the second emitter region.

18. A memory device comprising:

at least one thyristor having thyristor body regions including first and second immediately adjacent base regions respectively coupled to and between first and second emitter regions;

a first control port configured and arranged to capacitively couple a first signal at least to the first base region;

a first circuit configured and arranged to detect a temperature-related failure of the thyristor to maintain its conductance state during a standby mode or to maintain its blocking state;

and a second circuit including a second control port configured and arranged for receiving a second signal generated outside of the thyristor and for coupling the second signal at least to the second base region as a function of the detected failure for controlling holding current or forward blocking voltage of the thyristor;

wherein the second control port extends over a junction between the first and second base regions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jerome Jackson Jr. whose telephone number is 571-272-1730. The examiner can normally be reached on M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jj

JEROME JACKSON
PRIMARY EXAMINER